PATENT ABSTRACTS OF JAPAN

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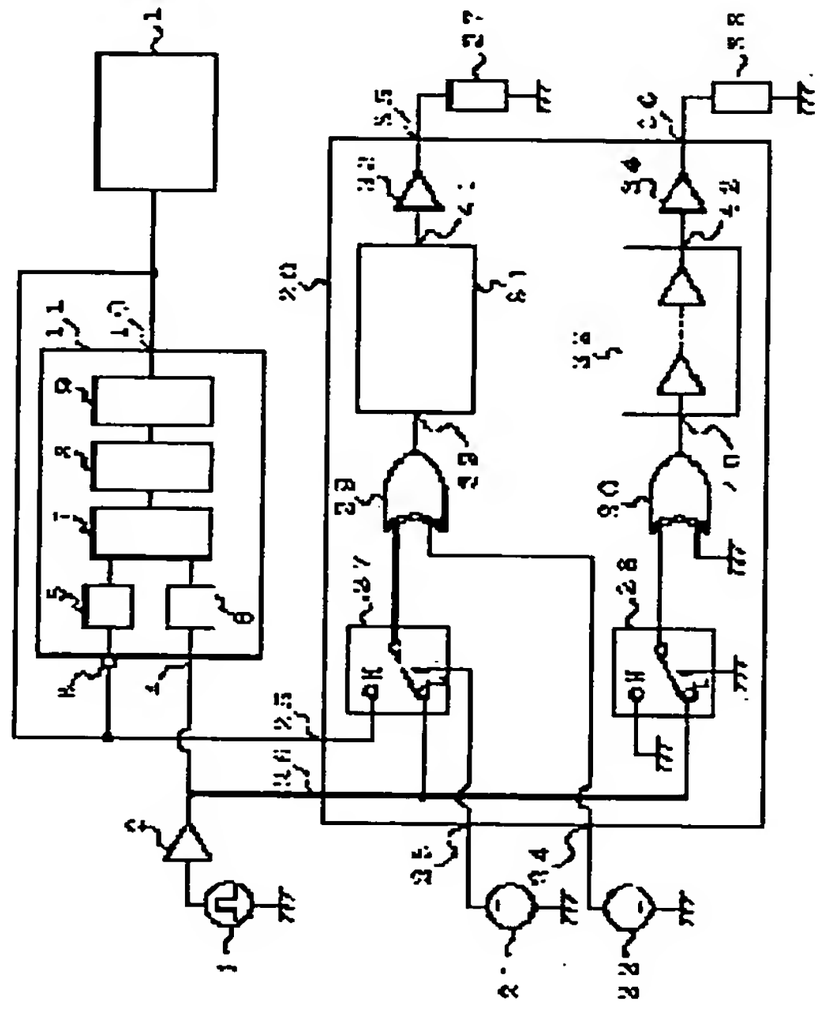
(54) CIRCUIT AND METHOD FOR MEASURING PHASE OFFSET

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce a measurement error resulting from a wiring path and to measure a phase offset with high precision by outputting the output signal of a phase-locked loop(PLL) circuit to a 2nd output terminal through a selector circuit when a 1st control voltage has a 2nd level.

SOLUTION: The selector circuit 27 is controlled by a voltage source 21 connected to a control terminal 23 and selects and outputs the signal from an input terminal 26 when the voltage of the voltage source 21 has a logical level (L) and the signal from an input terminal 25 when a logical level (H). Then the output terminal 10 of the PLL circuit 11 is connected to the input terminal 25 of a phase offset measuring circuit 20 and the input terminal 4 of the PLL circuit 11 is connected to the input terminal 26 of the phase offset measuring circuit 20, which measures a phase offset by measuring the phase of a reference signal and a clock signal outputted to the output terminal 35 and the phase of a reference signal outputted to an output terminal 36 by an external measuring instrument.



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